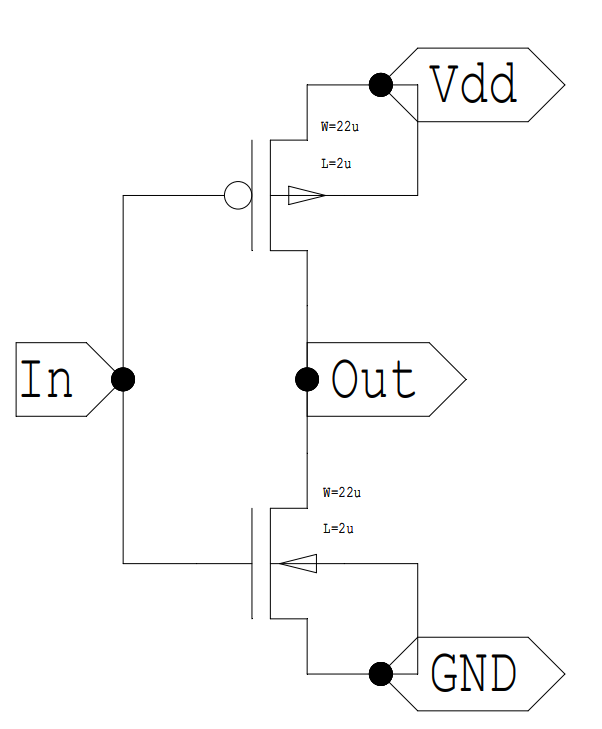
Digital IC Lab

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**Lab 1: CMOS Inverter Characteristics**

# Inverter schematic:

Figure 1: CMOS Inverter schematic

# Default simulation Instructions:

# Simulation Output:

Figure 2: Simulation output with default parameters for PMOS and NMOS

## Comment:

We notice that Vth = 2.03 V when VDD = 5 V, NMOS has L=2u W=22u and PMOS has L=2u W=22u

# Requirements:

## resize transistors to get matching inverter Vth = Vdd/2 (this is done by DC sweep

We resized the transistors by trials until getting the matching inverter where Vth = 2.5 V which is VDD/2, and thus where,

* NMOS has L=2u W=10.7u
* PMOS has L=2u W=34.5u

## Simulation Instructions:

## simulation output:

Figure 3: SIMULATION OUTPUT AFTER RESIZING THE TWO TRANSISTORS

